



Shipping Formal semantics and proof techniques for optimizing VHDL models FORMAL SEMANTICS AND PROOF TECHNIQUES FOR OPTIMIZING VHDL MODELS Kothanda Umamageswaran Sheetanshu L. Pandey Philip A. Wilsey Images for Formal Semantics and Proof Techniques for Optimizing VHDL Models This paper presents a formal model of the dynamic semantics of VHDL using . optimization techniques for improving the performance of VHDL simulators can To support this claim we present a proof asserting the validity of process-folding. Formal Semantics and Proof Techniques for Optimizing VHDL Models Formal semantics and proof techniques for optimizing VHDL models, Collectif, Springer Libri. Des milliers de livres avec la livraison chez vous en 1 jour ou en